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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/040,505	12/28/2001	Kevin X. Zhang	P11682	2608

25694 7590 10/06/2004

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EXAMINER	
CONNOLLY, MARK A	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 10/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/040,505	ZHANG ET AL.	
	Examiner	Art Unit	
	Mark Connolly	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-11,13-17 and 19-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-11,13-17 and 19-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6-10-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-3, 5-11, 13-17 and 19-21 have been presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 6-11 and 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over George et al [George] US Pat No 6785829 in view of Schutz et al[1] [Schutz] US Pat No 5440520.

4. Referring to claim 1, George teaches the processor substantially including:

a. a first port to receive a plurality of supply voltages from at least one external voltage regulator, each of the plurality of supply voltages to power a particular portion of the processor [245 and 255 fig. 2 and fig. 3]. Although it appears that the voltage being supplied to the processor through lines 245 and 255 are via separate ports, it is obvious that the two could be combined into a single port in order to reduce the number of ports being tied to a voltage regulator and which could be used to serve a different function.

b. a second port to provide a plurality of control signals to the at least one voltage regulator, each of the plurality of control signals to indicate a supply voltage [237 fig. 2 and col. 3 lines 46-54].

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[1] As cited in the previous Office Action

George does not explicitly teach that the processor comprises a plurality of voltage sensors, each to monitor one of the plurality of supply voltages and that the voltage sensors provide control signals to indicate if a respective supply voltage is above or below a target value.

Schutz teaches voltage sensors which monitor supply voltages and provide control signals to indicate if a respective supply voltage is above or below a target value [col. 7 lines 42-55]. A normal operating range is interpreted as being a target value and indicating if a supply voltage is either in or near an inoperable or destructive range identifies whether the voltage is above or below that normal operating range. It would have been obvious to include the voltage sensor taught by Schutz into the George system wherein each supply voltage would have its own voltage sensor in order to monitor and help provide an accurate supply voltage to each of the different portions of the processor [col. 7 lines 50-51].

5. Referring to claim 2, George teaches that at least one of the target values is adjustable in accordance with a power management policy [col. 5 lines 44-47].

6. Referring to claim 3, George teaches that the power can be adjusted in order to increase performance [col. 5 lines 44-47]. It is well known in the art that increased performance directly translates into increased speed. Increasing the speed of the processor is interpreted as meeting and maintaining a timing requirement required by the increased performance state of the processor.

7. Referring to claim 6, George teaches that the core is powered by one of the plurality of supply voltages [fig. 3 and col. 5 lines 44-47].

8. Referring to claims 7 and 8, George teaches that a memory region is powered by one of the plurality of supply voltages [fig. 3 and col. 5 lines 44-47]. The cache is interpreted as the memory region.

9. Referring to claims 9-11 and 13-15, George and Schutz teach the system and therefore also teach the method performing the functions of the system.

10. Referring to claim 16, George teaches electrically coupling a voltage supply output of a voltage regulator to a voltage supply input of a processor [fig. 2].

11. Referring to claim 17, George teaches electrically coupling a voltage supply control output of a processor to a voltage supply control input of a voltage regulator via a multiplexer [fig. 2].

12. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over George and Schutz as applied to claims 1-3, 6-11 and 13-17 above, and further in view of Shingo et al[2] [Shingo] EP 0872790.

13. Referring to claim 5, the George-Schutz system does not explicitly teach that the voltage sensor includes an op amp. In fact, the George-Schutz system does not explicitly teach anything that is included in voltage sensor except only that the voltage sensor compares the input voltage to the required voltage of the system [col. 7 lines 46-51 *in Schutz*]. Shingo teaches a means to compare an input voltage to a reference voltage using an op amp [col. 3 line 18-col. 4 line 3]. The comparators in Shingo are interpreted as op amps. Shingo explains that by using the op amps the system can monitor whether or not the supply voltage has deviated from a reference

[2] As cited by the applicant

voltage. It would have been obvious to one of ordinary skill in the art at the time of the invention to include the Shingo op amps into the George-Schutz system because the George-Schutz system requires a means to compare voltages and Shingo teaches a system to provide those means.

14. Claims 19-21 rejected under 35 U.S.C. 103(a) as being unpatentable over George and Schutz as applied to claims 1-3, 6-11 and 13-17 above, and further in view of Gupta et al [Gupta] US Pat No 5996083.

15. Referring to claim 19, although the George-Schutz system teaches varying the voltage to portions of the processor in order to conserve power, it is not explicitly taught that the adjustments are in response to a portion being inactive. Gupta teaches that power consumption of idle portions of a processor should be reduced [col. 1 lines 28-32, 38-47 and col. 2 lines 21-26]. It would have been obvious to one of ordinary skill in the art to reduce the voltage being supplied to inactive portions of the processor because it allows the power consumption of needless components to be reduced or eliminated without effecting system performance as taught by Gupta.

16. Referring to claims 20-21, these are rejected on the same basis as set forth hereinabove. George, Schutz and Gupta teach the system and therefore teach the method performing the functions of the system.

17. Claims 1-3, 6-11, 13-17 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta as cited above, in view of Schutz.

18. Referring to claim 1, Gupta teaches the processor substantially including:

a. a first port to receive a plurality of supply voltages to power a particular portion of the processor [figs. 1-2, col. 1 lines 28-32, col. 2 lines 40-44 and col. 7 lines 56-61]. Although Gupta does not explicitly teach an external voltage regulator, it is explicitly taught that power is controlled to particular portions of the processor and voltage regulators are a well-known means to supply controlled power and therefore would be obvious to include in the Gupta system.

b. a second port to provide a plurality of control signals to the at least one voltage regulator, each of the plurality of control signals to indicate a supply voltage [figs. 1-2, col. 1 lines 28-32 and col. 2 lines 40-44].

Gupta does not explicitly teach that the processor comprises a plurality of voltage sensors, each to monitor one of the plurality of supply voltages and that the voltage sensors provide control signals to indicate if a respective supply voltage is above or below a target value.

Schutz teaches voltage sensors which monitor supply voltages and provide control signals to indicate if a respective supply voltage is above or below a target value [col. 7 lines 42-55]. A normal operating range is interpreted as being a target value and indicating if a supply voltage is either in or near an inoperable or destructive range identifies whether the voltage is above or below that normal operating range. It would have been obvious to include the voltage sensor taught by Schutz into the Gupta system wherein each supply voltage would have its own voltage sensor in order to monitor and help provide an accurate supply voltage to each of the different portions of the processor [col. 7 lines 50-51].

19. Referring to claim 2, because the voltages to the processor portions are adjustable, it is obvious that the target values would also be adjustable to reflect the change in voltage.

20. Referring to claim 3, it is well known in the art that voltage and frequency have a direct relationship with each other and therefore when the target value is set it is inherent that it is set in order to satisfy a timing requirement.

21. Referring to claim 6, Gupta teaches that the portion of the processor could be units for performing functions or tasks [col. 5 lines 47-57]. A processor core is interpreted to be a unit for performing functions or tasks.

22. Referring to claims 7 and 8, Gupta teaches that the portion of the processor could be a cache [col. 5 lines 47-57].

23. Referring to claims 9-11 and 13-15, Gupta and Schutz teach the system and therefore also teach the method performing the functions of the system.

24. Referring to claim 16, it is obvious that in the Gupta-Schutz system that the voltage supply output of a voltage regulator would be electrically coupled to a voltage supply input of a processor in order to provide voltage power to the processor.

25. Referring to claim 17, it is obvious that in the Gupta-Schutz system that the voltage supply control output of a processor would be electrically coupled a to a voltage supply control input of a voltage regulator in order to provide power control signals to the voltage regulator.

26. Referring to claim 19, Gupta teaches that power consumption of idle portions of a processor should be reduced [col. 1 lines 28-32, 38-47 and col. 2 lines 21-26].

27. Referring to claims 20-21, Gupta and Schutz teach the system and therefore also teach the method performing the functions of the system.

28. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta and Schutz as applied to claims 1-3, 6-11, 13-17 and 19-21 above, and further in view of Shingo et al[3] [Shingo] EP 0872790.

29. Referring to claim 5, the Gupta-Schutz system does not explicitly teach that the voltage sensor (38) includes an op amp. In fact, the Gupta-Schutz system does not explicitly teach anything that is included in voltage sensor (38) except only that the voltage sensor compares the input voltage to the required voltage of the system [col. 7 lines 46-51]. Shingo teaches a means to compare an input voltage to a reference voltage using an op amp [col. 3 line 18-col. 4 line 3]. The comparators in Shingo are interpreted as op amps. Shingo explains that by using the op amps the system can monitor whether or not the supply voltage has deviated from a reference voltage. It would have been obvious to one of ordinary skill in the art at the time of the invention to include the Shingo op amps into the Gupta-Schutz system because the Gupta-Schutz system requires a means to compare voltages and Shingo teaches a system to provide those means.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark Connolly whose telephone number is (703) 305-7849. The examiner can normally be reached on M-F 8AM-5PM (except every first Friday).

[3] As cited by the applicant & above

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C Lee can be reached on (703) 305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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September 16, 2004

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